I feel that we are long due to update you on the development status of our e/c module. The first 20 PCBs arrived from China about a week ago and I decided to solder a few of them myself. This is very relaxing process (well not necessary for your eyes :) ). In about 3.5 hrs, I had 4 fully soldered boards ready for testing.

As usual, I used water-soluble flux, so at the end a quick bath in hot water made all 4 boards shiny ;).

But, let me go back to the actual design.

The echo cancellation chip is “placed” inline with a PCM stream (in it’s path). Basically, every voice fame goes through the chip while our driver decides if the e/c is to be performed or not (bypass mode). To talk to a chip’s registers we use CPU’s parallel bus. The silicon comes from Zarlink , well known Telecom chip manufacturer.
Zarlink provides several families of the LEC chips in various sizes and with various features. After some research and exchanging several emails with Zarlink’s FAE, we have decided to focus on two lines which are backwards compatible (well, almost 100%).
The ZL502xx series is the older group of chips which provides 4-32 channels with the same pinout. The second, newer generation family of chips ZL380xx provides almost the same pinout with similar capabilities plus an advanced noise matching technology. APIs are almost identical, only the addressing mechanism is slightly different but we take care of that inside our driver and the
CPLD
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At that point, I started working on a verilog code. Just to remind you, the Verilog is a hardware description language which creates images to “instruct”
CPLD
and
FPGA
chips on how to “behave”.

After taking a quick “refreshment course” and a couple of hours, the code was ready for both types of Zarlink chips.

At this point my focus shifted towards a software portion of this project..
More on this in the next post, please stay tuned.

Cheers,
Mark